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An FPGA-Based Digital Class-D Amplifier Using Short Word-Length

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Abstract— A digital Class-D amplifier based on single-bit processing to be implemented on a Field Programmable Gate Array (FPGA) is presented. The main focus of this design is the reduction of noise, a drawback of Class-D amplifiers, by exploring the noise-shaping characteristics of Sigma-Delta Modulation (SDM). The audio signal is retained in the digital single-bit domain until the final stage of the amplifier, thus avoiding quantization noise due to conversion. This paper focuses on the SDM and digital signal processing (DSP) components of the design to be implemented on the FPGA.

Keywords—Class-D, Sigma-Delta Modulation, FPGA, VHDL.

I. INTRODUCTION

Class-D amplifiers use PWM (pulse-width modulation) as the preferred modulation technique as it achieves minimal noise due to its low pulse switching frequency. Despite this, PWM has not been suitable for high-end audio applications due to its inability to provide a sufficient dynamic range and low signal-to-noise ratio (SNR). Pulse Density Modulation (PDM) has not been considered competitive for these applications either, because of its higher output pulse rate which results in additional noise. However, higher order Sigma-Delta modulators have shown that this noise can be further pushed out of the band of interest, making them an attractive choice for high-end audio applications.

Sigma-Delta Modulators provide an effective method to reduce noise in audio sampling applications by being able to shape the noise. SDM in combination with oversampling of the input signal can effectively shift much of the quantization noise out of the band of interest [1]. This is in contrast to traditional multi-bit sampling where quantization noise is spread evenly across the band of the signal. Additionally, in multi-bit systems the only method to lower the quantization noise is by increasing the number of bits, which is computationally expensive.

The approach suggested in this paper is unique to the extent that the signal is retained in the digital single-bit domain throughout the processing stages. This ensures that there is no distortion added due to multiple A/D and D/A conversions. The implementation complexity is simplified by incorporating DSP components on the FPGA, rather than using dedicated Digital Signal Processors. The Sigma-Delta Modulator shown in Fig. 2 is re-configurable to cater for different PCM standards including 16-/18-/20-/24-bit with sampling rates of 32 / 44.1 /

48 / 88.2/ 96 / 192 KHz which are common standards used in CD and DVD audio. For Super Audio CD (SACD), the SDM stage can be bypassed as the stream is already Sigma-Delta modulated. The design takes advantage of the research undertaken in the short word-length domain to implement algorithms such as DC blocking [2] and filtering [3].

The remainder of this paper is organized as follows. Section-II describes the overall function of the Class-D amplifier. In Section-III, the Sigma-Delta modulator and its ability to reshape the quantization noise have been discussed. Section-IV presents the implementation details of the components, while Section-V presents the experimental and simulation results. Finally, the paper concludes in Section-VI.

II. ARCHITECTURE

Figure 1. Functional Diagram of Class-D Amplifier

Fig.1 shows the functional diagram of the Class-D amplifier. The FPGA drives a pair of MOSFETs through a driver chip followed by an analog Low Pass Filter (LPF) and the speaker to complete the circuit [4]. The driver chip has high and low side outputs to drive the pair of push-pull power MOSFETs.

The signal is tapped at various points through the output stage to sense faults such as over-voltage, over-current, over-temperature, switching faults and presence of direct current (DC). The sensor signals are suitably conditioned to be fed to the FPGA, which also controls the overall operation of the amplifier. Fig.2 shows the block diagram of the complete Class-D amplifier. The Audio Input block represents the 16-bit

Pulse Code Modulation (PCM) encoded words sampled at a rate of 44.1 KHz. The 64x Interpolator oversamples the audio signal, which helps achieve excellent resolution and a high SNR in the band of interest.

Figure 2. Block Diagram of the Class-D Amplifier

The interpolator increases the frequency spectrum of the input signal to 2.82 MHz as shown in Fig.3. The Sigma-Delta Modulator performs the conversion of the PCM signal to a bitstream as required by the proposed Class-D amplifier design. The SDM is in effect a Digital-to-Analogue Converter (DAC) as it transforms a multi-bit signal to a PDM bitstream of 1's and 0's proportional to the input signal. In order to retrieve the original signal, the SDM bitstream is fed to an analogue LFP.

Figure 3. Oversampling and Downsampling Ratios

Before the SDM bitstream is passed to the driver chip, it needs to be downsampled to 400 KHz, failing which the thermal junction temperature of the driver IC will be exceeded [5]. Hence a 7:1 downsampler (refer to Fig. 3) is used in this case to band-limit the 2.82 MHz signal to 400 KHz. For other audio input formats, the ratio is suitably altered to ensure that the output is always band limited to 400 KHz.

The downsampled SDM signal passes through a Synchronizing block. The SDM bitstream is converted to a pair of complementary signals as required by the push-pull switching stage. Also, the output electronics requires that the system must maintain a minimum time between switching of these complimentary signals [6]. This is to ensure that both the MOSFETs do not conduct at the same time, which can produce a current that can be fatal for the transistors.

A Control Finite State Machine (FSM) as shown in Fig.4 is used to ensure proper operation of the amplifier. After the reset period, the FSM checks for power by reading flags from different sensors. Before entering the Sample Audio state, where it starts reading the PCM information, the FSM waits for a finite number of clock pulses (equivalent to 2 seconds),

which is a prerequisite for proper functionality of the driver IC [5]. The FSM also constantly monitors for a number of error conditions. If an error occurs, both MOSFETs are turned off and the audio signal is no longer sampled.

Figure 4. State Diagram of the Control FSM.

The basic error conditions include over-voltage (OVP), over-current (OCP), and over-temperature (OTP). A switching check error condition is triggered if either of the MOSFETs fails. A DC error condition is triggered if DC is detected at the input of the speaker. This is to protect the magnet-coil speaker from direct current, which has the potential to destroy the speaker voice-coil due to overheating.

The 'Sensors and Signal Condition' block consists of sensors to determine the aforementioned fault conditions. The signals from these sensors are suitably conditioned so that they can be fed to the FPGA. The Switching Output Amplification stage consists of a pair of power MOSFETs in a push-pull configuration. The MOSFETs are used to amplify the differential bitstream from the FPGA to useful power levels that can drive the speaker.

III. SIGMA-DELTA MODULATION AND NOISE SHAPING

Figure 5. Linear Model of First-Order SDM

A Digital First Order SDM sampled data equivalent block diagram is shown in Fig.5. The quantization noise e_n is modeled as an additive white noise signal. In order to understand the noise shaping characteristics of SDM, we start with the noise power for a *Nyquist rate* PCM quantizer.

Considering e_n to be white Gaussian noise, the power of which is given by:

$$\sigma_e^2 = \frac{\Delta^2}{12} \approx \left(\frac{2V}{2^N} \right)^2 / 12 \quad (1)$$

where V is the maximum quantized output value, N is the number of bits, and Δ represents the quantization step (i.e., $\Delta = 2V/(2^N - 1)$) [1].

If the signal is treated as a zero mean random process and its power σ_p^2 , then the signal to quantization noise ratio in dB is:

$$SNR = 10 \log \left(\frac{\sigma_p^2}{\sigma_e^2} \right) = 10 \log \left(\frac{\sigma_p^2}{V^2} \right) + 4.77 + 6.02 \quad (2)$$

when the PCM signal is oversampled i.e. sampled at a rate much higher than Nyquist rate, the noise σ_{eb} in the band of interest, f_B , is given by

$$\sigma_{eb}^2 = \frac{\sigma_e^2}{(osr)} \quad (3)$$

where oversampling ratio $osr = fs/(2f_B)$. As some of the noise power is located outside of the signal band, the maximum achievable SNR in dB is then:

$$SNR = 10 \log \left(\frac{\sigma_p^2}{\sigma_e^2} \right) = 10 \log(\sigma_p^2) - 10 \log(\sigma_e^2) + 10 \log(osr) \quad (4)$$

Taking the oversampling ratio as power-of-2 values, i.e., $osr = 2^\lambda$, we obtain

$$SNR = 10 \log(\sigma_p^2) - 10 \log(\sigma_e^2) + 3.01\lambda (dB) \quad (5)$$

implying that for every doubling of the oversampling ratio, i.e., for every increment in λ , the SNR improves by about 3 dB. The output of the first-order SDM shown in Fig.5 can be given by

$$s_n = p_{n-1} + e_n - e_{n-1} \quad (6)$$

Now, considering the SDM case, the in-band noise power at the output of a *first-order* SDM [1] is

$$\sigma_{eb}^2 = \sigma_e^2 \frac{\pi^2}{3} \left(\frac{1}{osr} \right)^3 \quad (7)$$

Thus, the SNR in dB for $osr = 2^\lambda$, is

$$SNR = 10 \log(\sigma_p^2) - 10 \log(\sigma_e^2) - 10 \log \left(\frac{\pi^2}{3} \right) + 9.03\lambda \quad (8)$$

Hence, for every doubling of the oversampling ratio, i.e., for every increment in λ , the SNR improves by 9 dB.

Adopting the same approach, the ideal formula of in-band SNR for an M^{th} order Sigma-Delta modulator is given as

$$SNR = 10 \log(\sigma_p^2) - 10 \log(\sigma_e^2) - 10 \log \left(\frac{\pi^{2M}}{2M+1} \right) + (20M+10) \log(osr) (dB) \quad (9)$$

which implies that the in-band quantization noise is reduced by $3(2M+1)$ dB for every doubling of the osr [7]. Hence, using oversampling ratio $osr = 64$ and a 5th order Sigma-Delta modulator gives a theoretical SNR of 198 dB, although practical limitations would impose a more realistic value of around 100 to 150 dB.

However, modulators of order higher than two are considered inherently unstable [8] and have to be modified to function as desired. The approach suggested in [9] [10] was used to design a stable 5th order Sigma-Delta Modulator.

IV. IMPLEMENTATION

Figure 6. The Fifth Order SDM

The design shown in Fig.6 uses feed-forward and leaky feedback to stabilize the modulator. The output from stages 2, 4 and 5 is fed back via $a1$, $a2$ and $a3$. As the feedback is leaky, the values of $a1$, $a2$ and $a3$ are in the range of 0.001 [9], [10] (as shown in Table I). The output of the modulator is the weighted sum of the outputs of each Sigma-Delta stage.

TABLE I. OPTIMIZATION OF 5th ORDER SDM COEFFICIENTS

Coefficient	Actual	Approx to	%Rounding
a1	0.001	1/1024	2.34
a2	0.0015	1/512	30.20
a3	0.0017	1/512	14.88
b1	547	512	6.39
b2	244	256	4.91
b3	62.2	64	2.89
b4	7.1	8	12.67
b5	1	1	0

The output coefficients $b1$, $b2$, $b3$, $b4$, and $b5$ determine the contribution of the corresponding stage to the overall output. In order to ensure that the modulator is never driven into saturation, the output of stage 2 is compared with a fixed reference to determine whether it would drive the proceeding stages into saturation. If the output of stage 2 is greater than twice the maximum input value (or less than twice the minimum input value), the integrators in stages 3, 4 and 5 are reset. It is important to remember that since $b1 \gg b2 \gg b3 \gg b4 \gg b5$, the outputs of stages 1 and 2 contribute the most to the output at any time.

The implementation of the SDM requires many multipliers and dividers if the coefficients presented in [9] [10] are used. In order to optimize the design, the feed-forward and feedback coefficients are approximated to their closest power-of-2 values as shown in Table I. This facilitates multiplication and division to be replaced by bit-shifting, thus significantly reducing the logic required. The optimization achieved by this method can be seen in Table II.

Figure 7. Synchronizing Block

The Sigma-Delta modulated pulses are downsampled to 400 KHz and fed to the synchronizing block shown in Fig.7. The input 'SDM_DS' to the block is converted to a differential signal 'LO_OP' and 'HI_OP', which drive a pair of MOSFETs. Also, a finite delay is maintained between the switching of these signals which ensures that both the MOSFETs are not turned on at the same time. This is achieved

by delaying the bitstream by a number of clock pulses before generating the required differential signals. Although the switching delay is constant, the actual number of flip-flops in the chain varies with the operating frequency of the system. The differential output is shown in Fig.8.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. FPGA Implementation Results

The FPGA implementation results of the 5th order SDM, downsampler, Control FSM and the Synchronizer are shown in Table II. The results of the original and approximated coefficients are listed along with the optimization achieved.

TABLE II. SYNTHESIS RESULTS

ALTERA EP2C35	Actual Coeff	Approx Coeff	Optimization
No. of Logic Elements	1401	338	75.87 %
No. of Registers	173	179	- 3.4 %
No. of M4Ks	8	8	0 %
No. of RAM bits	36,864	36,864	0 %
No. of LABs	173	29	83.23 %
Max. Frequency	26.42 MHz	112.25 MHz	85.83 MHz

An Altera Cyclone-II FPGA is used to implement the digital components of the amplifier along with a 32 Kbit ROM that stores a PCM audio file. With the actual coefficients for the 5th order SDM, the design occupies a total of 173 Logic Array Blocks (LABs) and operates at 26.42 MHz, narrowly meeting the frequency requirements for 64x oversampling of DVD Audio (24.57 MHz). However, with the approximated power-of-2 coefficients, only 29 LABs were used by the design and the maximum operating frequency is 112.25 MHz. However, the number of registers used was slightly less in the actual coefficient design due to the combinational nature of the multipliers and dividers used.

B. Simulation Results

Figure 8. Output of the Synchronizer (FPGA) on a CRO

The methodology used to test the SDM uses a combination of MathWorks Matlab and Mentor Graphics ModelSim simulations. Matlab is used to generate a 16-bit PCM input signal to the SDM which is written out to a text file. This file is then read by the VHDL SDM design. After each input has been processed, the output is written out to a text file. Matlab code for an analog LPF is used to demodulate the SDM bitstream.

Figure 9. PCM Input, SDM Output and Demodulated SDM Waveforms

Figure 10. PCM Input and Demodulated SDM Spectra

Fig.9 shows the Matlab waveforms of the original PCM, the single-bit SDM output and the demodulated SDM. It can be seen that the demodulated output signal is time-shifted from the original input signal due to the initial tracking delay of the SDM. Fig.10 shows a 10 KHz input signal along with the demodulated SDM output which demonstrates the SNR performance of the system.

The SNR of the system is determined by comparing the SNR of the input signal to the SNR of the demodulated output signal. By comparing these two SNR values the true SNR of

the system is deduced. For instance, the five-run average of the in-band input SNR is 16.34 dB, whilst the in-band output SNR averaged 16.45 dB. These results show that the SDM reduces noise in the input signal band, by pushing it out of the band of interest.

In this simulation a DC blocker from [2] is incorporated to reflect the complete system, the effects of which are apparent in Fig. 10. It eliminates the unwanted DC component and further improves the SNR at the output. In this DC-blocker, both the input and the output are in single-bit format. It is designed using a Delta modulator topology with Sigma-Delta Modulation embedded in its feedback path.

VI. CONCLUSION

The proposed digital Class-D amplifier aims to reduce noise in high end audio applications by minimizing the quantization noise. Multi-bit PCM input to the system is converted to the single-bit domain using a reconfigurable Fifth Order SDM. The SDM is optimized for hardware implementation by approximating the feedback and feedforward coefficients. This results in a significant improvement in logic utilization and frequency of operation.

The testing has shown that the designed SDM achieves a good SNR in the band of interest and also provides high fidelity. Future work includes interfacing the FPGA with the output electronics and analyzing the performance of the entire system for SNR, Total Harmonic Distortion (THD), audio fidelity and quality.

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